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EXAMINER	
NGUYEN, DUC M	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/743,218	Applicant(s) DUPUIS, TIMOTHY J.
	Examiner DUC M. NGUYEN	Art Unit 2618

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-18 and 20-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-18,20-25,29-33 and 38-47* is/are rejected.

7)☒ Claim(s) *26-28 and 34-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to applicant's response filed on 2/6/08. Claims 1, 3-18, 20-47 are now pending in the present application.

Claim Rejections - 35 USC ϶ 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1, 3, 16, 18, 24, 25, 29-31, 38-42, 47** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Jensen** (US 5,159,283) in view of **Blake** (US 6,847,904).

Regarding claim **1**, **Jensen** discloses an RF apparatus formed using an integrated circuit, comprising :

- an power amplifier circuitry formed using the integrated circuit (see col. 1, lines 46-47), wherein it would have been obvious to one skilled in the art to integrate the power amplifier as well as the power control circuit in a single IC package as disclosed by **Blake** (see Fig. 1 and Abstract), for utilizing advantages of IC such as size and cost; and

- circuitry formed using the integrated circuit for generating a power ramp profile to control the output power of the RF power amplifier (see col. 1, lines 37-51 and Fig. 1, wherein sequence of values representing ramp-up and ramp-down waveforms stored in ROM 14 would read on the claimed ramp profiles).
- a digital interface for providing interface between the IC and an external controller (see Fig. 1 and col. 3, lines 25-42), where it is clear that all the input signals (power control data, transmit and clock) are digital signals. Therefore, any one of the references 10, 12, 14, 16 would read on the claimed "digital interface", and the transmit controller (not shown) would read on the claimed "external controller".

Therefore, the claimed limitations are made obvious by Jensen in view of Blake.

In an alternative way, **Blake** would teach all the claimed limitations (see Figs.1-2 and related disclosures) except for a power amplifier and ramp profiles. However, **Jensen** teaches a power amplifier and ramp profiles. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify Blake for storing ramp profiles in the memory shown in Fig. 1 of Blake and further incorporating a ramp generator to generate a gain control according to a selected ramp profile as claimed, for further improving the performance of the amplifier.

Regarding claim **3, Jensen** fails to teach a serial interface. However, **Blake** teaches a serial interface for controlling a gain of a power amplifier (see Fig. 1 and col. 5, line 45 – col. 6, line 43). Since one skilled in the art would recognize the benefit of the serial interface circuit in **Blake** for controlling the amplifier gain (see Blake, col. 1, lines 53-

63), it would have been obvious to one skilled in the art at the time the invention was made to modify Jensen for further providing a serial interface as claimed, for minimizing pin count of the amplifier IC package (see Blake, col. 5, lines 55-60).

Regarding claim **16, 25,** the claims are rejected the same reason as set forth in claim 1 above. In addition, **Jensen** would teach a digital to analog converter circuit (18) formed using the integrated circuit for generating a power control signal based on generated ramp profiles (see Fig. 1, ref. 18).

Regarding claims **18, 24,** the claims are rejected the same reason as set forth in claim 1 above. In addition, **Jensen** would teach a plurality of stored ramp profiles and a selection stored at the IC as claimed (see col. 3, line 25 – col. 4, line 36).

Regarding claim **29**, the claim is rejected the same reason as set forth in claim 18 above. However, Jensen does not explicitly teach the transmit controller (not shown) is a baseband controller. However, it is noted that utilizing such a baseband controller for controlling the power of a power amplifier is well known in the art (Official Notice). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify Jensen for utilizing a baseband controller as a transmit controller as well, so that a gain control processing as well as a baseband processing could be utilized with single DSP located at the baseband controller, for cost saving (see also Blake, Fig. 2).

Regarding claims **30-31,** the claims are rejected the same reason as set forth in claim 29 above. In addition, **Jensen** as modified would teach a digital serial interface located between the baseband controller and the integrated circuit (see Blake, Fig. 2).

Regarding claim **38**, the claim is rejected the same reason as set forth in claim 29 above. In addition, it would have been obvious to one skilled in the art at the time the invention was made to modify Jensen to integrate the transmit controller in a second IC circuit as well, for utilizing advantages of an IC circuit such as size and cost.

Regarding claims 39-40, the claims are rejected the same reason as set forth in claim 38 above. In addition, since the use of either GaAs substrate or silicon substrate for amplifiers is well known in the art, it would have been obvious to one skilled in the art at the time the invention was made to further modify Jensen for providing substrates as claimed, for utilizing advantages of each substrate such as cost and/or performance quality.

Regarding claim 41, the claim is rejected the same reason as set forth in claim 38 above. In addition, it would have been obvious to use a printed circuit board as claimed, for utilizing advantages of the printed circuit board such as easy interface connection.

Regarding claim 42, the claim is rejected the same reason as set forth in claim 38 above. In addition, it would have been obvious to use a substrate as claimed, for utilizing advantages of the substrate such as low power dissipation.

Regarding claim **47,** the claim is rejected the same reason as set forth in claim 38 above. In addition, **Jensen** would teach a digital to analog converter circuit (18) formed using the integrated circuit for generating a power control signal based on generated ramp profiles (see Fig. 1, ref. 18).

4. Claims **20-21, 32** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Jensen** in view of **Blake** and further in view of **Richard** et al (US 6,894,266).

Regarding claims **20-21, 32**, **Jensen** as modified fails to teach one or more sensors in the IC. However, since utilizing a temperature sensor on an amplifier IC circuit is known in the art as disclosed by **Richard** (see Fig. 3), it would have been obvious to one skilled in the art at the time the invention was made to modify Jensen for providing a temperature sensor in the IC circuit as well, for temperature compensation purpose, for further improving the performance of the amplifier.

5. Claims **22-23, 33** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Jensen** in view of **Blake** and **Richard** and further in view of **Lin** et al (US 2004/0038701).

Regarding claim 22, **Jensen** as modified fails to teach a ramp profile for battery voltage. However, since **Lin** also discloses a ramp profile for battery voltage (see [0004]), it would have been obvious to one skilled in the art at the time the invention was made to further incorporate the above teaching Lin to Jensen for providing a voltage sensor and a ramp profile based on voltage information as claimed, for stabilizing the gain control caused by voltage level changes.

Regarding claim 23, 33, **Jensen** as modified would teach the ramp profile is selected based on a power control signal and a sensed property as claimed.

6. Claims **1, 3, 16** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Bell** (US 5,642,075) in view of **Blake** (US 6,847,904).

Regarding claim **1**, **Bell** discloses an RF apparatus formed using an integrated circuit (see col. 2, lines 23-37), comprising

- an amplifier circuitry formed using the integrated circuit (see Fig. 1 and col. 2, lines 23-37) and
- circuitry for generating a power ramp profile to control the output power of the RF power amplifier (see Fig. 1, wherein the ramp generator would read on the ramp profile).

Although **Bell** does not specifically disclose the amplifier is the power amplifier, one skilled in the art would recognize that an power amplifier would work equally well with Bell's teaching. Therefore, the claimed limitation regarding the power amplifier is made obvious by Bell.

As to the newly added limitation regarding a digital interface for providing an interface between the power amplifier circuit and an external controller, it is noted that the logical circuits in Figs. 6A, 6B of Bell are digital interfaces (see Figs. 6A, 6B), and that the Vref as shown in Fig. 1 of Bell for controlling the gain of the amplifier would obviously be a digital signal as an external controller for controlling the amplifier to a desired output level in the similar way as disclosed by **Blake** (see Fig. 1 and col. 6, lines 20-24). Therefore, the claimed limitation regarding the newly added limitation is made obvious by Bell, in view of Blake.

Regarding claim **3,** it is clear that the digital interface would comprise serial interfaces (see also Blake, Abstract).

Regarding claim **16,** Bell discloses a digital to analog converter circuit (17) formed using the integrated circuit for generating a power control signal based on generated ramp profiles (see Fig. 1, ref. 17).

7. Claims **1, 3-14, 16-17, 38-47** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Lee** (US 2003/0152056) in view of **Lin** (US 2004/0038701) and **Blake** (US 6,847,904).

Regarding claim **1**, **Lee** discloses an RF apparatus formed using an integrated circuit (see Fig. 3B or 4A), comprising

- an power amplifier circuitry formed using the integrated circuit (see [0045] regarding “on-chip” limitation which implies an integrated circuit as well) and
- circuitry for generating a power control signal to control the output power of the RF power amplifier (see [0049]).

Although Lee is silent on a ramp profile, it is clear that the power control signal in Lee would obviously be based on a ramp profile as disclosed by Lin (see [0004], 0005]). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the above teaching Lin to Lee for providing a ramp profile as claimed, so that power control based on a ramp profile according to a transmission condition could be selected for controlling amplifier gain, for further improving the performance of the AGC.

As to the newly added limitation regarding a digital interface for providing an interface between the power amplifier circuit and an external controller, it is noted that Lee in view of Lin would teach an external controller for the power amplifier. Here, although Lee as modified fails to disclose a digital interface for the power amplifier circuit, it is noted that using such a digital interface for controlling the gain of an amplifier is known in the art as disclosed by **Blake** (see Fig. 1 and Abstract). Since Lee teaches a power manage unit 447 that "provides power management features that are controlled through setting of the power management registers". This **register** feature clearly suggests digital signals for the settings, not to mention many digital serial interfaces for the wireless IC circuits are disclosed through out the **Lee** reference, and since one skilled in the art would recognize the benefit of the PGA IC package in **Blake** (see col. 1, lines 53-63), it would have been obvious to one skilled in the art at the time the invention was made to incorporate the above teaching Blake to Lee for providing a digital interface to the amplifier as well, for minimizing pin count of the amplifier IC package (see Blake, col. 5, lines 55-60).

Regarding claim **3,** it is clear that Lee as modified would disclose the digital interface comprises a serial interface as claimed (see Blake, Fig. 1 regarding the SPI reference).

Regarding claims **4-6**, since **Lin** discloses a ramp profile for temperature gain control (see [0004]), this would implicitly require a temperature sensor for measurement. Therefore, Lin would disclose one or more sensor and one or more ramp profile based on information from the sensor. Since controlling amplifier based on temperature information is well known in the art, it would have been obvious to one skilled in the art

at the time the invention was made to incorporate the above teaching Lin to Lee for providing a temperature sensor and a ramp profile based on temperature information as claimed, for stabilizing the gain control caused by temperature changes.

Regarding claim 7, since Lin also discloses a ramp profile for battery voltage (see [0004]), it would have been obvious to one skilled in the art at the time the invention was made to further incorporate the above teaching Lin to Lee for providing a voltage sensor and a ramp profile based on voltage information as claimed, for stabilizing the gain control caused by voltage level changes.

Regarding claim 8, since using an external control signal for controlling amplifier based on transmission mode (analog mode or digital mode) is known in the art (Official Notice), and since Lin also discloses a plurality of stored ramp profiles for selecting a ramp profile based on transmission conditions such as temperature, voltage of a battery, and transmission frequency (see [0004]), it would have been obvious to one skilled in the art at the time the invention was made to further modify Lin and Lee for providing an external control signal to control the amplifier based on transmission mode or transmission frequency (i.e, transmission frequency for analog mode and transmission frequency for digital mode are different), and in combination with information from one or more sensors as well, for further improving the performance of the AGC.

Regarding claims 9-10, since Lin also discloses a processor (see Fig. 1 or 3), which may be a DSP (see [0006]) for controlling amplifier gain, it would have been obvious to one skilled in the art at the time the invention was made to further

incorporate the above teaching Lin to Lee for providing a DSP to control the amplifier gain as well, so that a plurality of ram profiles could be generated by the DSP for controlling amplifier gain, for further improving the performance of the AGC. By doing so, the DSP in view of Lee would be formed using the integrated circuit (see Fig. 4A wherein the baseband processor and RF transceiver are all integrated on a single IC).

Regarding claims 11-12, the external control signal is rejected for the same reason as set forth in claim 8 above.

Regarding claim 13, it is clear that Lee in view of Lin would teach a serial interface using the integrated circuit for downloading ramp profiles (see Lin, [0018]) onto the integrated circuit (see Lee, Fig. 3A, [0053]).

Regarding claim 14, it would have been obvious to one skilled in the art that the timing control unit 506 in Fig. 5 of Lee would provide a clock signal for the DSP in order to synchronize operations of the DSP and other I/O interfaces.

Regarding claim 16, Lin discloses a DAC as claimed (see Fig. 1, ref. 114)

Regarding claim 17, it is clear that Lee in view of Lin would teach the RF apparatus comprises memory formed using the integrated circuit, wherein the memory stores a plurality of ramp profiles for controlling the output power of the power amplifier.

Regarding claim 38, the claim is rejected the same reason as set forth in claim 1 above, wherein the “on-chip” amplifier would read on the “first integrated circuit”, the “WLAN transceiving integrated circuit” for controlling amplifier power would read on the “second integrated circuit” (see [045], [0049]).

Regarding claims 39-40, the claims are rejected the same reason as set forth in claim 38 above. In addition, since the use of either GaAs substrate or silicon substrate for amplifiers is well known in the art, it would have been obvious to one skilled in the art at the time the invention was made to further modify Lee for providing substrates as claimed, for utilizing advantages of each substrate such as cost and/or performance quality.

Regarding claim 41, the claim is rejected the same reason as set forth in claim 38 above. In addition, it would have been obvious to use a printed circuit board as claimed, for utilizing advantages of the printed circuit board such as easy interface connection.

Regarding claim 42, the claim is rejected the same reason as set forth in claim 38 above. In addition, it would have been obvious to use a substrate as claimed, for utilizing advantages of the substrate such as low power dissipation.

As to claims 43-47, Lin would disclose sensors, DSP, ram profiles and DAC for the same reason as set forth in claims 4-8, 16 above (see also Fig. 1 and [0018]).

8. Claims **15, 28** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Lee** in view of **Lin** and **Blake**, and further in view of **Yu et al** (US 5,365,190).

As to claims 15, 28, the claims are rejected the same reason as set forth in claim 14 above. However, Lee fails to disclose the clock signal is generated by dividing the RF input signal. However, Yu discloses an RF device wherein the clock signal is generated by dividing the RF input signal. Therefore, it would have been obvious to

one skilled in the art at the time the invention was made to provide Yu's teaching to Lee, to generate the clock signal by dividing the RF input signal as well, for cost saving.

Allowable Subject Matter

9. Claims 26-28, 34-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

As to claims 26, 34, the cited prior art fails to teach an apparatus or method for controlling the output power of the RF power amplifier which comprises components and steps as specified in the claim, wherein a non-obvious feature comprises a digital signal processor and profiles which are located at the IC circuit for selecting a ramp profile to control the output power of the RF power amplifier based on a digital control signal received from a controller that is external to the IC circuit.

Response to Arguments

11. Applicant's arguments filed 2/6/08 have been fully considered but they are not persuasive.

In the response filed 2/6/08, Applicant contends that

Bell discloses an amplifier circuit using an automatic gain control (AGC). The circuit of Bell is designed to adjust the gain of amplifier 14 so that the output Vout is maintained at a desired RMS value. Bell uses a reference voltage Vref to maintain the RMS value of Vout. In the example provided, Bell states that 2Vref is equal to 2 Volts. (Col. 3, line 61). Blake discloses a programmable gain amplifier. Blake discloses an external analog reference voltage Vref that is connected to a gain setting resistor ladder network 112.

Applicant asserts that, in both Bell and Blake, Vref is not a digital signal. Vref in both patents is described as a voltage reference. One typical definition of a voltage reference is a fixed/constant voltage irrespective of the loading of a device, power variation, and temperature. This is different from a digital signal, which is a signal in which discrete steps are used to represent information, commonly using binary codes (l's and O's). Further, Bell even teaches that Vref can be proportionally reduced to compensate for loss. It is unclear how a digital signal can be proportionally reduced, if it can only have a "high" or "low" value. Applicants request that the Examiner explain how the reference voltages in Bell and Blake are digital signals.

In response, the Examiner asserts that both Bell and Blake do not teach the reference voltage Vref is an **analog** signal, noting that Applicant has failed to provide any paragraph in Bell's or Blake's references that would support his/her allegation that the reference voltage Vref is an **analog** signal. In fact, since the reference voltage Vref is just a desired output power level, one skilled in the art would recognize that such reference value would be a digital value stored or programmed in a memory of a controller/processor. Here, the examiner can not think of a situation in which a reference voltage would be an analog signal (how ?). For example, even though the amplifier requires an analog bias voltage to operate, such analog bias voltage would be fixed at a maximum operation voltage and would be adjusted by a digital control signal to adjust resistors or the likes (i.e, utilizing a voltage divider) to provide a desired bias voltage to the amplifier.

As to Applicant's argument that "It is unclear how a digital signal can be proportionally reduced, if it can only have a "high" or "low" value. Applicants request that the Examiner explain how the reference voltages in Bell and Blake are digital signals". In response, the Examiner asserts that a reference voltage such that 8V when programmed or stored in a memory of a controller would represent in the digital format as "1000" (a well known decimal to binary conversion in computer literature), and when the 8V is reduced to 6V, the digital format for 6V would be "0110", not just "high" or "low" as alleged by Applicant.

Since the logical circuits in FIGS. 6A and 6B of Bell are digital circuits, it is believed that the Vref is a digital signal (a binary representation of a decimal number). Further, the digital signal processor in Fig. 2 of Blake's reference clearly suggests that a digital control signal is inputted to the amplifier.

Applicant further contends that

As discussed above, amended claim 1 recites a power amplifier formed using the integrated circuit, circuitry for generating a power ramp profile formed using the integrated circuit, and a digital interface for providing an interface between the integrated circuit and an external controller. As argued above, Applicants assert that the voltage references (Vref) are not digital interfaces. The Office Action also relies on logical circuits in Figs. 6A and 6B of Bell as digital interfaces, and ramp generator 24. However, claim 1 recites that the digital interface provides an interface between the integrated circuit and an external controller. Using the Office Action's interpretation of Bell, the logical circuits in FIGS. 6A and 6B do not appear to provide an interface with an external controller, since the ramp generator and power amplifier would be formed using the same integrated circuit. FIGS. 6A and 6B of Bell show the gain latch, ripple counter, delay and reset control circuitry shown in FIG. 1. It is unclear how these could be an interface that meets the requirements of amended claim 1.

In response, the Examiner asserts that even though the ramp generator and power amplifier would be formed using the same integrated circuit, this does not imply that the Vref is not controlled by an external controller. In fact, Fig.2 in Blake clearly suggests a DSP as an external controller and that Vref could be an internal or an external parameter (see col. 6, lines 20-24). Note that the serial peripheral input (SPI) for controlling offset calibration, bandwidth, power utilization of the amplifier in Blake (see col. 5, lines 48-50) are also external digital inputs received from an external controller such as DSP, PLA, ASIC or like (see Blake, col. 6, lines 34-42).

Applicant further contends that

Lee discloses a wireless local area network (WLAN) transceiving integrated circuit (IC), including a WLAN interface, an input buffer and controller, and a processor. An IC of Lee (e.g., IC 350 of FIG. 3B) includes a

power amplifier 352, core components 351, and serial and parallel interfaces 320 and 324 to interface with a host 322. An IC of Lee (e.g., IC 400 of FIG. 4A) may include a baseband 404. Lee does not appear to teach or suggest, however, an integrated circuit with a digital interface for providing an interface between the integrated circuit and an external controller, wherein the digital interface is a digital interface for receiving a digital signal from an external controller, and wherein the digital signal contains power control data. The interface between the power amplifier 352 and the core components 351 (FIG. 3B) appears to include an transmit signal TX and an non-digital power control signal TX_PC. There also appears to be no teaching in Lee that the interfaces 320 and 324 (FIG. 3B) provide an interface for a digital signal that contains power control data.
Lin discloses a wireless transmission apparatus used for transmitting an RF signal. Like Lee, Lin also does not teach or suggest an integrated circuit with a digital interface for providing an interface between the integrated circuit and an external controller, wherein the digital interface is a digital interface for receiving a digital signal from the external controller, and wherein the digital signal contains power control data. The power amplifier 118 receives an RF input signal R118 and an analog control signal from the power control loop 116.
For at least these reasons, applicant asserts that amended claim 1 is allowable over the cited prior art. Since dependent claims 3-17 depend from amended claim 1, it is also believed that these claims are allowable over the prior art.

In response, <u>the Examiner asserts that **Lee** does not teach the power control signal TX_PC is an **analog** signal, noting that Applicant has failed to provide any paragraph in Lee's references that would support his/her allegation that the power control signal is an **analog** signal</u>. In fact, in paragraph [0053], Lee teaches a power manage unit 447 that "provides power management features that are controlled through setting of the power management registers". <u>This **register** feature clearly suggests digital signals for the settings, not to mention many digital serial interfaces for the wireless IC circuits are disclosed through out the **Lee** reference.</u> Since one skilled in the art would recognize the benefit of the PGA IC package in **Blake** (see col. 1, lines 53-63), it would have been obvious to one skilled in the art at the time the invention was made to incorporate the above teaching **Blake** to **Lee** for providing a digital serial interface for controlling the power amplifier gain as well and would work equally well, for minimizing pin counts of the amplifier IC package (see Blake, col. 5, lines 55-60).

By doing so, the transmission power control TX_PC in Lee as modified would be inputted as a serial data input SI in Blake for controlling the gain of the power amplifier (see Blake, col. 5, line 45 - col. 6, line 7).

Applicant further contends that

Claim 18 recites a method of amplifying RF signals comprising "providing an RF power amplifier formed on an integrated circuit," "storing a plurality of ramp profiles in the integrated circuit," "receiving one or more digital control signals containing power control data from a controller that is external to the integrated circuit, wherein the control signals are received over a digital interface," and "selecting one of the ramp profiles to vary the output power of the RF power amplifier based on a desired output power level relating to one or more of the digital control signals from the controller."

When rejecting claim 18, the Office Action states that "Lin discloses a plurality of stored ramp profiles and a selection as claimed (see [0018])." However, Lin does not teach or suggest storing the ramp profiles on an integrated circuit, and receiving digital control signals containing power control data from a controller that is external to the integrated circuit.

As to claim 18, the arguments are rendered moot in view of the new ground of the rejection.

Applicant further contends that

Amended claim 38 recites an RF power amplifier module comprising "power amplifier circuitry formed using a first integrated circuit," "control circuitry formed using a second integrated circuit," "a digital interface formed using the first integrated circuit, wherein the digital interface is configured to allow digital power control signals from an external controller to be received by the power amplifier circuitry," and "memory formed using one of the first and second integrated circuits, wherein a plurality of ramp profiles are stored in the memory for varying the output power of the power amplifier circuitry based on desired output power levels relating to one or more of the digital power control signals received from the external controller."

When rejecting claim 38, the Office Action states that claim 38 is rejected for the same reason as claim 1, "wherein the 'on-chip' amplifier would read on the 'first integrated circuit', the 'WLAN transceiving integrated circuit' for controlling amplifier power would read on the 'second integrated circuit' (see [045], [0049])." Using this interpretation of FIG. 3A of Lee, the power control signal TX_PC would have to be the "digital power control signal." Applicant can find no evidence in Lee that the power control signal TX_PC is a digital signal. Also, when Lee describes other interfaces in FIG. 3A that are digital interfaces (interface 320, 324, 308, etc.), Lee explicitly does so. This is appears to be further evidence that signal TX_PC is not a digital signal.

In response, the Examiner asserts that Lee in view of Lin and Blake would teach the power control signal is a digital signal. In fact, any gain control signal output from a DSP or a baseband controller would be a digital signal. This digital signal would then be inputted to the serial data input SI in Blake for controlling the gain of the amplifier. Here, by simply incorporating a memory storing with ramp profiles in Lin to a controller in Lee for improving the gain performance, and utilizing the PGA IC circuit in Blake for the power amplifier in Lee for minimizing pin counts of an IC package, Lee as modified in view of Lin and Blake would teach all the claimed limitations of claim 38.

Applicant further contends that

Claim 29 recites a method of controlling a wireless communication device comprising "providing a baseband controller," "providing an integrated circuit having an RF power amplifier, memory, a digital interface, and an RF input, all formed using the integrated circuit," "storing a plurality of ramp profiles in the memory formed using the integrated circuit," "sending a digital power control signal from the baseband controller to the integrated circuit using the digital interface, wherein the digital power control signal relates to a desired output power level," "selecting one of the plurality of ramp profiles based on the digital power control signal received from the baseband controller," and "using the selected ramp profile to control the output power of the RF power amplifier."
As mentioned above, claim 29 has been rejected under § 103 as being unpatentable over Lee in view of Lin and Blake, and further in view of Gunzelmann. Lee, Lin, and Blake are discussed above. Gunzelmann discloses a transmission configuration for a mobile radio communication system. Gunzelmann shows an interface 2 that includes conductors 21, 22, 23, and 24. Conductor 21 carries a digital signal and is designed for transmission of the payload data which is provided from a digital signal processor. The module 3 (including the power amplifier 31) of Gunzelmann does not appear to receive an analog RF input signal to be amplified, but rather appears to receive a digital signal, which is converted into a signal to be amplified. Further, a combination of the cited references does not teach or suggest a method as recited in claim 29. For example, such a combination does not teach or suggest providing an integrated circuit having an RF power amplifier, memory, a digital interface, and sending a digital power control signal from the baseband controller to the integrated circuit using the digital interface.

As to claim 29, the arguments are rendered moot in view of the new ground of the rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See the attached PTO-892.

13. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for **formal** communications intended for entry)

(571)-273-7893 (for informal or **draft** communications).

Hand-delivered responses should be brought to Customer Service Window, Randolph Building, 401 Dulany Street, Alexandria, VA 22314.

Any inquiry concerning this communication or communications from the examiner should be directed to Duc M. Nguyen whose telephone number is (571) 272-7893, Monday-Thursday (9:00 AM - 5:00 PM).

Or to Nay Maung (Supervisor) whose telephone number is (571) 272-7882.

/Duc M. Nguyen/

Primary Examiner, Art Unit 2618

Apr 15, 2008